REMARKS

I. Formal Matters.

Claims 1-7, 9 and 12-13, and 15-25 are all the claims pending in the application, claims 24 and 25 newly added via this amendment. Applicant thanks the Examiner for acknowledging Applicant's claim to priority under 35 U.S.C. §119 and for confirming receipt of a certified copy of Applicant's priority document.

II. Claims.

The Examiner rejects claims 1, 16, 22 and 23 under 35 U.S.C. § 102(e) as allegedly being anticipated by *Tanaka et al.* (U.S. Patent No. 6,194,758).

Claims 1 and 16. The present invention relates to a method of manufacturing a system on chip semiconductor device that includes a CMOS logic circuit portion and a DRAM portion, which has a memory cell portion and peripheral portion, on a single semiconductor substrate. The peripheral portion of the DRAM portion includes an address decoder, a sense amplifier, and so on to perform data read and write operations on each memory cell of the memory cell portion. In accordance with the present invention, claims 1 and 16 require a method of manufacturing a transistor in the CMOS logic circuit portion, another transistor in the DRAM portion, and a memory cell with an HSG structure, all of which are formed on the single semiconductor substrate.

Tanaka explicitly shows in Fig. 18 and teaches a method of manufacturing a semiconductor device that has a memory cell region and peripheral circuit region. *Tanaka* teaches a memory cell region and a peripheral circuit portion of the DRAM portion but fails to teach or suggest a CMOS logic portion. The Examiner equates the peripheral circuit region of

Tanaka with the CMOS logic portion of the present invention (OA page 2). *Tanaka* teaches a general purpose DRAM that has a memory cell region and a peripheral circuit portion. At Figs. 18-20, *Tanaka* teaches and shows a method of fabricating *the second modification of the DRAM* according to a first embodiment (col. 20, lines 34-36). Thus, *Tanaka* fails to disclose an apparatus or method to manufacture a transistor in the CMOS logic circuit portion, another transistor in the DRAM portion, and a memory cell with and HSG structure on the single semiconductor substrate. At least for this deficiency, the rejection of claims 1 and 16 as being anticipated by *Tanaka* under 35 U.S.C. § 102(e), should be withdrawn.

Claim 22 is asserted as being allowable at least by virtue of its dependence upon an allowable claim.

The Examiner rejects claim 23 as being anticipated by *Tu* (U.S. Patent No. 6,200,898) under 35 U.S.C. § 102(e).

Claim 23 is cancelled without prejudice or disclaimer.

The Examiner rejects claims 2, 3, 17, 18, 20 and 21 under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Tanaka* in view of *Sung* (U.S. Patent No. 5,858,831).

Claims 2, 3, 17, 18, 20, and 21 are asserted as being allowable at least by virtue of their dependence upon an allowable claim.

The Examiner rejects claims 4-7, 9, 12-15, and 19 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Tanaka* in view of *Sung* as applied to claims 2, 3, 17, 18, 20, and 21, and further in view of AAPA (applicant's admitted prior art).

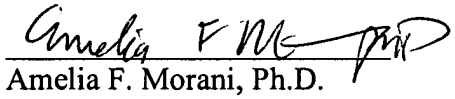
Claims 4-7, 9, 12-13, 15 and 19 are asserted as being allowable at least by virtue of their dependence upon an allowable claim.

Claim 14 is cancelled without prejudice or disclaimer.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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